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Hard macrocells for DC/DC converter in automotive embedded mechatronic systems

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Abstract

A novel configurable DC/DC converter architecture, to be integrated as hard macrocell in automotive embedded systems, is proposed in the paper. It aims at realizing an intelligent voltage regulator. With respect to the state of the art, the challenge is the integration into an automotive-qualified chip of several advanced features like dithering of switching frequency, nested control loops with both current and voltage feedback, asynchronous hysteretic control for low power mode, slope control of the power FET gate driver, and diagnostic block against out-of-range current or voltage or temperature conditions. Moreover, the converter macrocell can be connected to the in-vehicle digital network, exchanging with the main vehicle control unit status/diagnostic flags and commands. The proposed design can be configured to work both in step-up and step-down modes, to face a very wide operating input voltage range from 2.5 to 60 V and absolute range from -0.3 to 70 V. The main target is regulating all voltages required in the emerging hybrid/electric vehicles where, besides the conventional 12 V DC bus, also a 48 V DC bus is present. The proposed design supports also digital configurability of the output regulated voltage, through a programmable divider, and of the coefficients of the proportional-integrative controller inside the nested control loops. Fabricated in 0.35 μm CMOS technology, experimental measurements prove that the IC can operate in harsh automotive environments since it meets stringent requirements in terms of electrostatic discharge (ESD) protection, operating temperature range, out-of-range current, or voltage conditions.

Keywords: Embedded control systems, Architectures for DC/DC converters, Macrocells, Automotive electronics, Intelligent power management, In-vehicle networking

1 Introduction

Automotive electronic systems are evolving as a network of embedded control units (ECU) implementing sensor and/or actuator interfacing plus digital signal processing techniques for a wide range of applications. Embedded electronics is used both for non-safety-critical functions (e.g., infotainment, user interface, driver/passenger comfort) and for safety-critical ones such as the control of propulsion, transmission, steering, braking, and vehicle dynamics. For safety-critical applications, stringent requirements have to be met in terms of extended temperature range, electrostatic discharge (ESD) protection, diagnostic against out-of-range current, and voltage

or temperature conditions. Both high-voltage power electronic circuits and low-voltage signal processing and networking circuits have to be integrated within the same embedded mechatronic unit. Particularly, in emerging hybrid and electric vehicles, multiple voltage domains have to be managed [1–3]: 24 or 48 V for electric/hybrid propulsion and power-demanding mechatronic loads and 12 V for conventional on-board electronic sub-systems. From these values, also supply levels of few volts have to be generated for low-power components such as sensors and their analog and mixed-signal front-end, and digital circuitry for processing, memory, and networking. Due to phenomena like cranking at vehicle start or over-voltages, the input battery voltage can be reduced below 5 V or can increase up to 60 V. Therefore, both step-down and step-up capabilities are required to the DC/DC voltage regulation system.

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For example, Fig. 1 shows the block diagram of a new generation of starter/alternator systems for electric/hybrid vehicles, we recently proposed in [1], consisting of an embedded unit connected through a digital serial bus (Local Interconnect Network (LIN)) to the main vehicle control unit and receiving both 48 and 12 V power supplies. The 48 V value is used for the rotor excitation in the electrical machine, whereas the 12 V is used to supply the sensing and control circuitry. Classic solutions at the state of the art foresee the realization of separate boards for the power and the sensing/control parts. The DC/DC regulation system is usually realized using multiple commercial off-the-shelf (COTS) components, each implementing a specific function (e.g. step-up or step-down) for a specific voltage domain. However, this approach increases the size and cost of the mechatronic components.

Another key automotive application requiring configurable DC/DC converters is LED lighting: typically, strings of multiple LEDs are used where, depending on the type of light (front, rear, left, and right), and hence, the string length, an output voltage from few volts to tens of V is required. For example, a string of high brightness LED, each operating with 3 V forward voltage and 330 mA forward current, is adopted in ref. [4]. By properly regulating a 48-V output voltage, a string of 16 LEDs can be formed with an output power of 16 W/string. The same power level may be obtained by connecting in series 5 LEDs with 3 V forward voltage and 1 A forward current, see [5], requiring a regulated voltage of 15 V. The LED voltage regulator shall

be interfaced to the digital vehicle network (through LIN or CAN), to exchange status/diagnostic flags and commands with the main vehicle control unit (the same of Fig. 1) for intelligent lighting management [6].

Since automotive is a large volume market, a solution integrating the voltage regulation part with the low-power control/networking part can allow a reduction of the cost and the size of each unit, according to the evolution scheme presented in Fig. 2 with reference to an automotive starter/alternator unit. To this aim, in this paper, we present the design and experimental characterization of a hardware macrocell for switching-based voltage regulation, integrated in complementary metal-oxide semiconductor (CMOS) technology featuring:

- Management of large input voltage range from 2.5 to 60 V (with nominal inputs at 12, 24, or 48 V)
- Step-up and step-down conversion capability
- Programmable output voltage, which can be regulated from 1 to 48 V
- Advanced techniques such as hysteretic control for low-power consumption and frequency dithering for reduced electromagnetic interference emission
- Integrated diagnostic capability and macrocell interfacing through a digital bus

Hereafter, Sections 2 and 3 present the architecture of the DC/DC converter macrocell architecture, and the circuital implementation of its sub-blocks focusing on

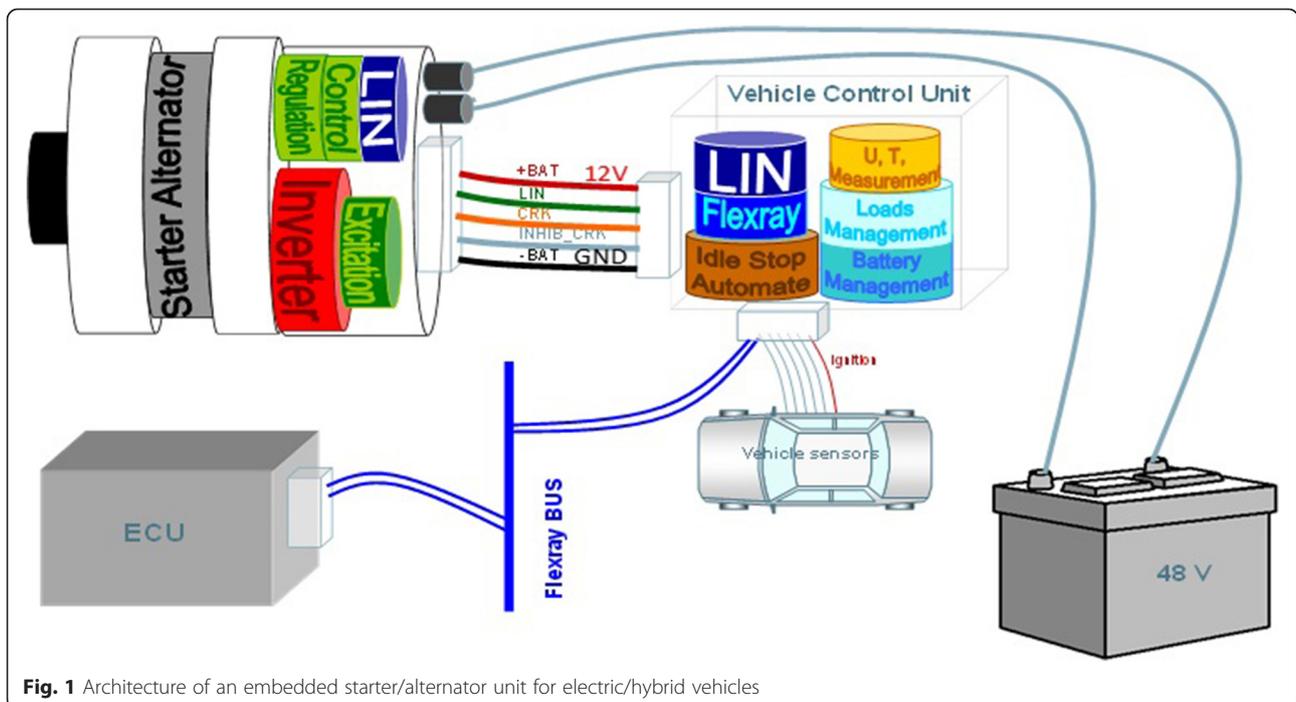


Fig. 1 Architecture of an embedded starter/alternator unit for electric/hybrid vehicles

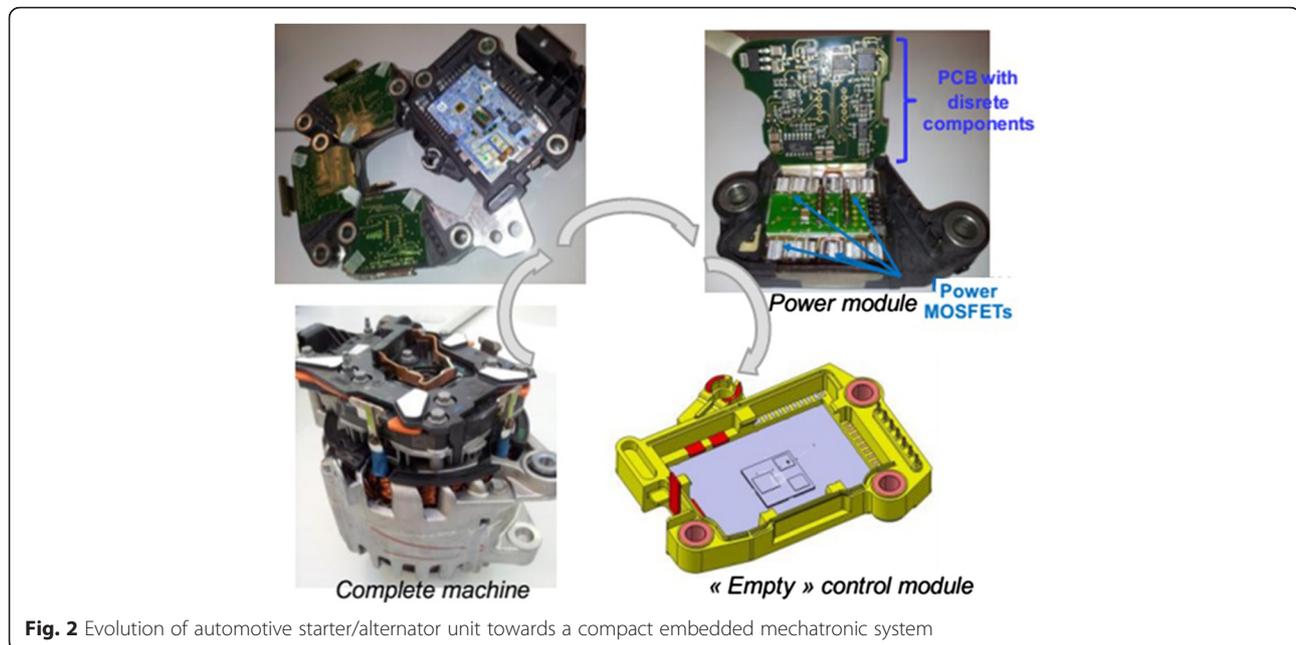


Fig. 2 Evolution of automotive starter/alternator unit towards a compact embedded mechatronic system

innovative features vs. the state of the art. Section 4 presents the implementation in CMOS technology, the experimental setup, and some of the performed measurements, and a comparison to the state of the art. Conclusions are drawn in Section 5.

2 Architecture of the integrated DC/DC converter

Designing integrated DC/DC converters operating in automotive environment is particularly challenging. Beside typical requirements of switching converters, like high power efficiency and good line/load regulations, also harsh specifications have to meet such as extended ambient operating temperature (from $-40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$), ESD protection up to 4 kV, reduced interference vs. other electronic devices, and wide input voltage range under or over the nominal battery voltage (e.g., from few volts in case of cranking up to max. 60 V in case of 48 V battery systems [1, 2]). The flexibility of the design is also a key issue since the same IC architecture should address different voltage supply specifications and converter topology: with galvanic isolation or not, step-up or step-down. The architecture we present has been integrated in a $0.35\text{ }\mu\text{m}$ CMOS technology from AMS AG, which allows for both low-voltage devices and high-voltage lateral diffused MOS transistors. The latter have been sized in this design to sustain a maximum voltage of 70 V. The key features of the smart DC/DC converter vs. state of the art [1, 7–9] are the digital programmability of the output voltage, the slope control of the MOS driver, the dithering of the frequency used in the PWM-like control loop, and the asynchronous hysteretic control which is activated when the load current is low to minimize the power consumption.

The above features allow to increase the flexibility of the DC/DC converter and to reduce the interference emission and the power dissipation.

The proposed converter can be configured to work both in step-up and step-down mode, and in case of problems, it can automatically switch from one mode to another (e.g. automatic switch from step-down to step-up mode in case of battery cranking). With respect to other works in literature [10–13], where smart DC/DC converter functionalities are verified by simulations, this work implements all the described features in a fabricated silicon prototype that was subject to a full experimental characterization.

The integrated power FET and power diodes are enough to sustain current levels of hundreds of milliamps (e.g., in case of automotive LED lighting applications). As example, in this work, the implemented prototype, experimentally characterized in Section 4, can sustain up to 0.9 A. In case of an embedded mechatronic system requiring multiple regulated outputs, with independent regulations to avoid single-point of failure according to automotive standards [3], an array of the same DC/DC converter hardware macrocell can be realized by proper scaling the integrated power FET area of each channel according to the maximum current to sustain.

Instead, in case of load current levels higher than 1 A (e.g., the rotor excitation current of an automotive starter/alternator amounts to several tens or few hundreds of amperes [14]), it is more convenient adding external power FET and power diode. In such case, the integrated converter acts as driver for the off-chip power FET. External components have to be used also for

capacitors and inductors (or transformers, depending if a galvanic isolation between the 48 V DC bus and the low voltage part is required).

Figure 3 shows the DC/DC converter with integrated FET, using a transformer for galvanic isolation between the 48 V DC domain and the output regulated domain. In Fig. 3, R_{sense} acts as current sensor. The scheme in Fig. 3 realizes a flyback converter, which is a galvanic-isolated topology with step-up and step-down capabilities. Since the power FET in Fig. 3 is switching, the current flowing in the series made by L_{pri} (the inductance at the primary side of the transformer) and by the FET is an AC current. Its waveform is shown in Fig. 3, with the label I_{pri} . According to the theory of primary-side regulated flyback converters [15], it is a train of triangular pulses (when the FET is “on”, there is the rising slope of the current). The AC signal is also present at L_{sec} , the inductance at the secondary side of the transformer, which is then rectified through the fast-switching diode D of Fig. 3 (this diode is integrated on chip). The output capacitance C_o in Fig. 3 implements a low-pass filtering effect to reduce the output ripple. Therefore, two conversions are implemented in the scheme of Fig. 3: first, a DC-AC and then an AC-DC, whereas between the primary and the secondary side of the transformer, there is an AC-AC coupling. An example of the same circuit, configured in boost topology, is showed in Fig. 5 in Section 3. In this case, there is also a first DC-AC coupling, since the FET in Fig. 5 is switching, and then a diode-based rectification implementing an AC-DC conversion.

As sketched in Fig. 3, the core of the DC/DC converter circuit can be divided into five main blocks, further detailed in Section 3: power management unit (PMU); DC/DC controller; FET gate driver; diagnostic block; and digitally programmable voltage divider. To be noted that Fig. 3 shows a configuration using an NMOS as power FET device, although the same DC/DC controller can produce outputs for a PMOS power FET with relevant FET gate driver (to be used when the integrated voltage regulator is configured as step-down without a transformer for galvanic isolation). For digital interconnection in Fig. 3, LIN is preferred vs. other automotive wired bus, like CAN or Flexray, since it allows for a maximum sustained bandwidth of 20 kbps, enough for the target application of this work, at reduced complexity and cost. LIN is a de facto standard in vehicle engineering for local interconnections [16].

3 Hardware macrocell details

3.1 On-chip PMU

The on-chip power management unit includes a low-drop out (LDO) regulator, a bandgap-stabilized voltage reference, and an integrated temperature sensor. The LDO regulator generates the internal supply voltage for the internal digital and analog blocks, including the gate drivers for P-channel and N-channel on-chip power FETs.

The main challenge for the PMU is to guarantee its functionality when the battery voltage falls down to 2.5 V. If such a voltage is applied, the driver is not able to turn the active element on and the functionality of the converter is lost. The flexibility of the PMU was

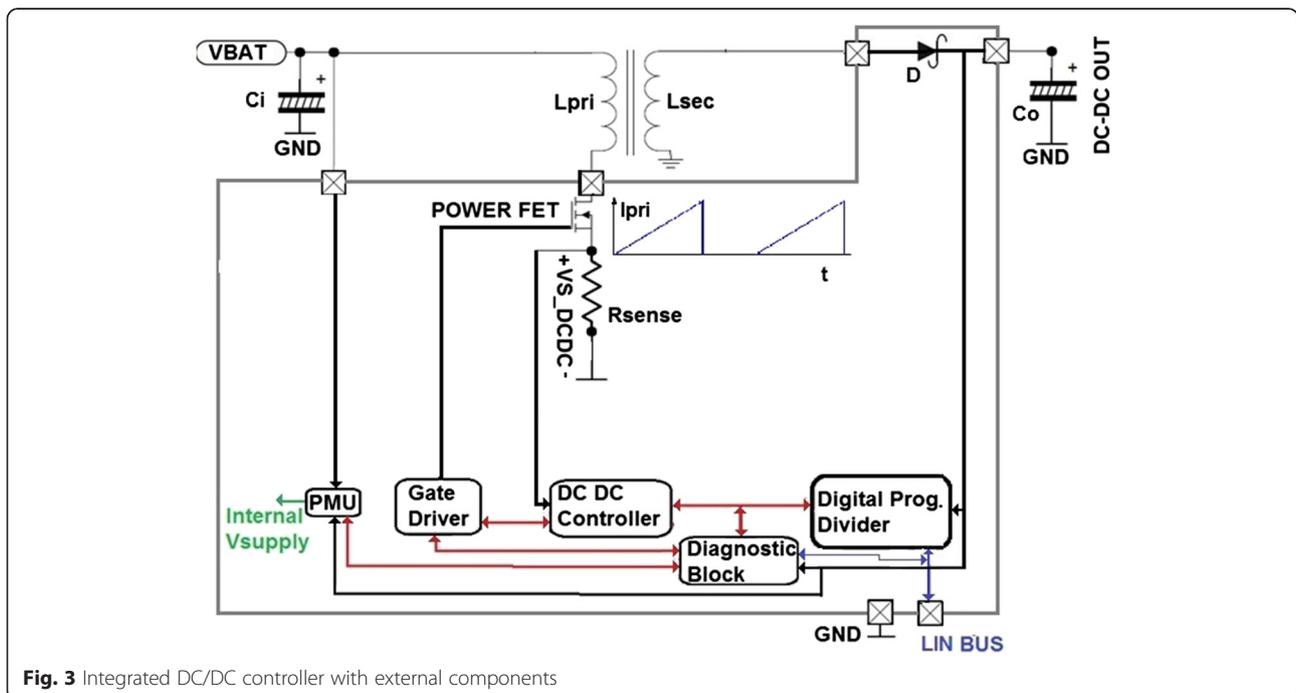


Fig. 3 Integrated DC/DC controller with external components

improved by implementing, see Fig. 4, a diode-based circuit able to switch the supply voltage of the PMU to the higher voltage between the battery voltage (VBAT) and the output of the converter. During the regular operating condition, the input voltage from the battery supplies the PMU, but when an undervoltage condition occurs (e.g., due to cranking) and the battery voltage drops down to a few volts, the system keeps working by switching the supply source of the PMU to the DC/DC output.

The bandgap stabilized reference voltage generates the internal reference for the DC/DC controller, see Fig. 5. A particular attention was paid to this block because the accuracy and the temperature drift of the regulated output voltage are directly connected to the performance of the bandgap. For the high voltage integrated bandgap, according to an IP reuse strategy, the hardware macrocell we already designed and verified through experimental measurements in [17] has been adopted.

The temperature sensor monitors the junction temperature of the IC and triggers an interrupt to the diagnostic block every time an over-temperature condition occurs by turning off the converter, according to the safety strategy of the chip.

3.2 DC/DC controller

The characteristics of a DC/DC converter mostly depend on the feedback control loop. In this work, considering all the different programmable conditions of the output voltage, the main challenges for the design of the control were

- to reach high performance in terms of efficiency, line regulation, and load regulation
- to reduce the power consumption when the load sinks a very low current

Hence, we implemented the following double-control strategy:

- i) Current mode control with two nested loops (current and voltage feedbacks) in normal conditions for better regulated performances

- ii) Hysteretic control in case of low load current for low-power operation

During the regular operation of the converter, to achieve good performance in terms of step response and in terms of line and load regulations, the control acts like a current-mode control [7, 8], with a switching frequency that can be configured up to 888 kHz. This current-mode control includes two nested loops, as shown in Fig. 5: the outer voltage loop (red) and the inner current control loop (green). The nominal frequency of the loop is programmable at 444 or 888 kHz. As further discussed in Section 3.6, to spread the electromagnetic interference caused by a pure synchronous converter, a dithering technique of the switching frequency is applied. The nominal output voltage is set through the digitally programmable resistive divider (PRD block of orange color in Fig. 5) integrated on-chip in the DC/DC converter macrocell. The divider generates two different voltage thresholds for every programmable value of the output voltage. The first threshold is the FB_THR and it is used for the regulation loop. The second threshold, the OS_THR, is used to clamp the output voltage reducing the overshoot of the output voltage during the startup of the system or during transient responses to variations of the input voltage or load current. Finally, the control generates a PWM signal driving the gate of the power FET. A proportional and integral (P.I. in Fig. 5) control function is applied within the voltage control loop to achieve the duty cycle modulation that regulates the output voltage to the nominal value. The coefficients of the P.I. can be configured to perform a flexible design, allowing to have a good trade-off between the regulation performance and the stability margin of the system in different conditions of the programmable output voltage.

The step responses of systems controlled through a P.I. function are often affected by overshoot. Even if the overshoot can be minimized in typical conditions properly configuring the P.I. coefficients, the process-voltage-temperature (PVT) spread can cause a higher overshoot in other operating conditions. As the target of the DC/DC converter is to work in the harsh automotive environment, it has to operate properly in a wide ambient temperature range. To solve this issue, a dedicated structure was added vs. the state of the art to the regulation loop to keep the overshoot under control. In Fig. 5, the overshoot is limited by the OS_THR produced by the digitally programmable divider. When the output voltage exceeds this threshold, the power FET is switched off and the overshoot is limited. When the regulated voltage begins to converge to the nominal value, the PWM signal is applied to the gate of the power FET again, and the regular operation is restored.

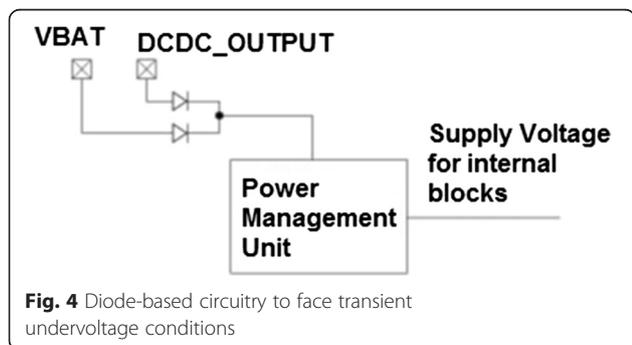
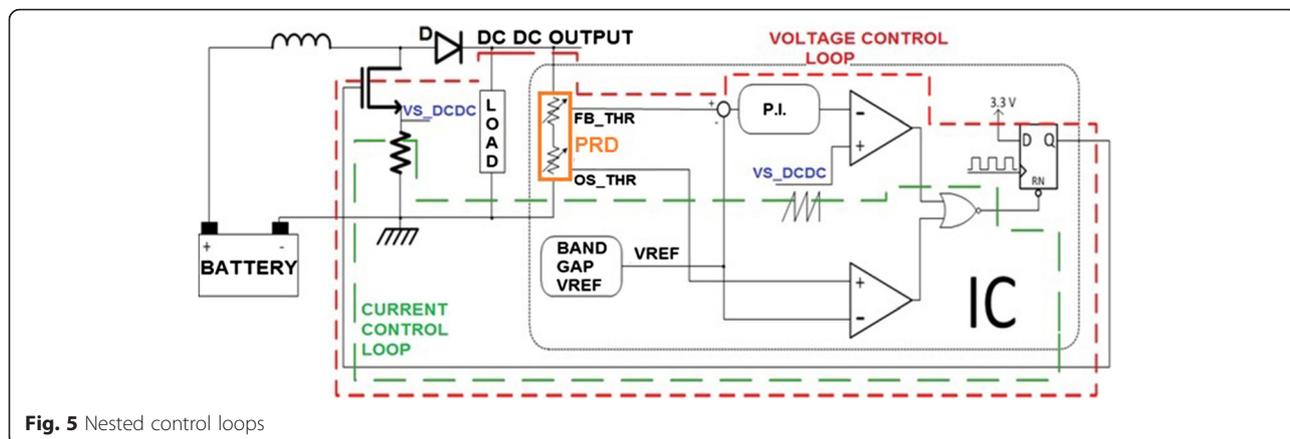


Fig. 4 Diode-based circuitry to face transient undervoltage conditions

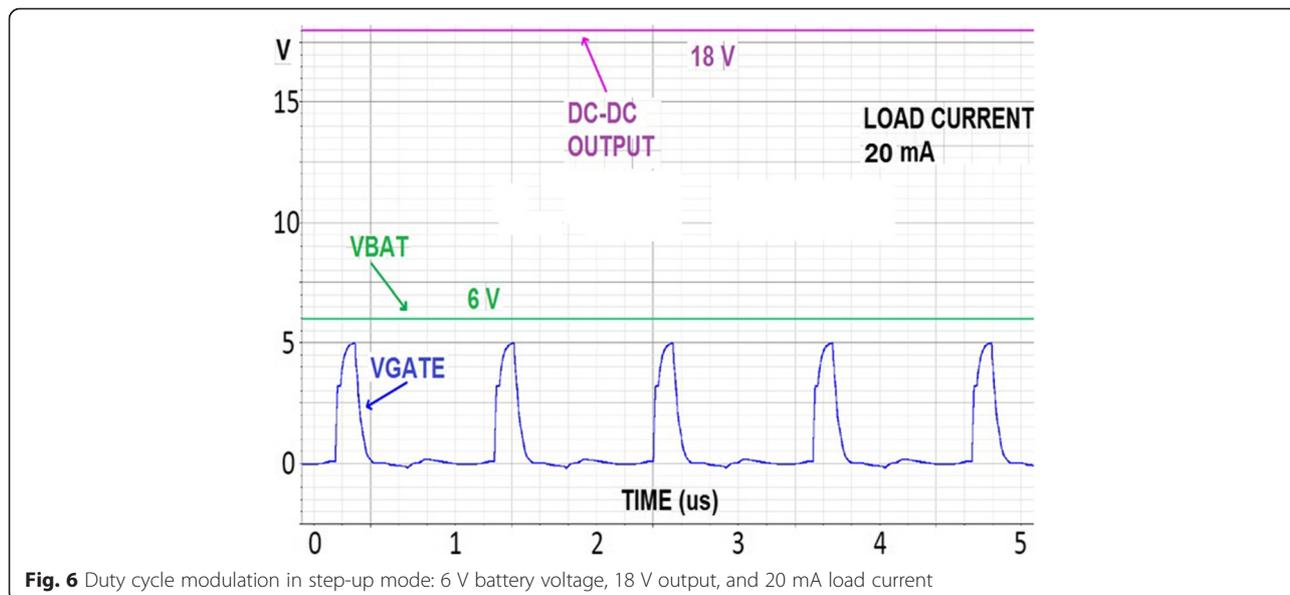


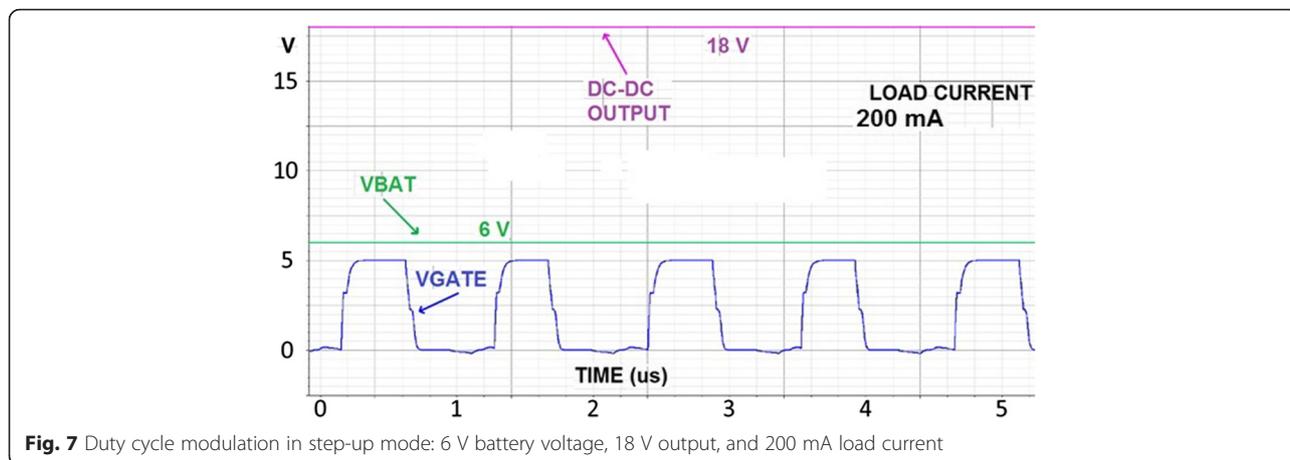
Figures 6 and 7 show how the modulation of duty cycle allows to compensate variations of the output current, keeping the output voltage stable to the desired value. In fact, in Fig. 6, the duty cycle is low as the converter is regulating to 18 V from a battery voltage of 6 V sourcing just 20 mA. Instead, in Fig. 7, the duty cycle is increased to supply a ten times greater current, 200 mA. Similar results are obtained for the compensation of variation of the input voltage. In Figs. 6 and 7, the DC/DC converter is configured in step-up mode. On the contrary, Fig. 8 shows an example of the DC/DC converter when used in step-down mode to regulate from 25 V battery voltage to a 18 V output voltage (with 200 mA load current).

The configurations in Figs. 7 and 8 are representative of automotive LED lighting applications with a string of 6 LEDs (each with 3 V forward voltage) when the input voltage falls down to 6 V (cranking) or grows to 25 V, e.g., due to overvoltage. To be noted that the waveforms in Figs. 6, 7, and 8 have been experimentally measured

using the fabricated IC prototype and the measuring test bed proposed in Section 4.

The low power hysteretic control was implemented to fulfill the challenging automotive requirements on power saving. This control by-passes the regular synchronous control, when the load current is low (e.g., during standby states or when the load is working with reduced performance). In this condition, it does not required a very accurate supply, and the power consumption is mainly low due to continuous charging/discharging the gate capacitance of the power FET while the conductive power losses are negligible (the load current is low). Since the hysteretic control is an asynchronous control, it avoids unnecessary switching activity and the converter can save power. Indeed, when the converter is in low power mode, the power FET is turned on only when the output voltage falls down the nominal output voltage value. Once the power FET is turned on, the converter keeps sourcing energy to the output until the output



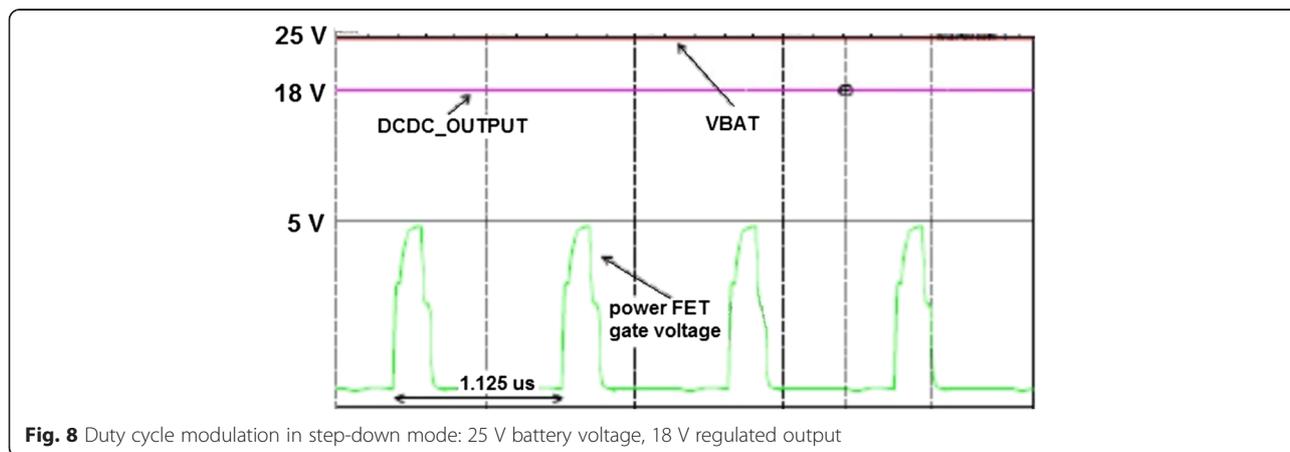


voltage reaches a value slightly greater than the nominal one. After that the switch is kept off until the load current has slowly discharged, the output capacitor behind the target value and the cycle starts again. Since in this condition, the current sunk from the DC/DC’s output port by the load is very low, the voltage on the output capacitor will take a long time to discharge, and hence, the hysteretic control allows to minimize the switching activity. In low power mode, the total current consumption of the IC is reduced at about 300 μ A, saving about the 80 % of the current consumption vs. the normal mode, which implements the nested control loops of Fig. 5.

3.3 Slope controlling of the power FET gate driver

The gate driver is the final stage of the control loop. It manages the turn-on and turn-off of the FET switch. In many applications, the gate driver is a simple CMOS inverter (i.e., a couple of a P-MOS, acting as a pull-up transistor, and an N-MOS, acting as a pull-down transistor with common input and output signals) with a size to have a current capability high enough to drive the input gate capacitance of the power FET at the desired switching

frequency. In automotive applications, instead, constraints on power dissipation and electromagnetic emissions make the design of this block much more challenging [18]. In our design, electromagnetic emissions are reduced by minimizing the cross conduction. Conventional CMOS inverter drivers are affected by cross conduction during the commutation of the output signal. During the transitions of the PWM signal, the cross conduction generates current spikes from the supply (VDD) to ground (GND) when the gate-source capacitor (C_{gs}) of the power transistor is charged and discharged. These spikes are periodical at twice the switching frequency of the converter. In the presented solution, the current spikes are minimized by minimizing the cross conduction of the gate driver. The concept behind the proposed gate driver is shown in Fig. 9. The input signal of the gate driver is V_{in33} . The signal V_{in33} is generated by the digital core of the IC, and it is immediately shifted from 3.3 to 5 V (V_{in}) to turn on the power switch having a $V_{gs_{on}}$ typically greater than 2.5 V. The first stage of the gate driver includes the two CMOS inverters I_1 and I_2 . These inverters are low-power inverters, and their function is to shape the input signal of



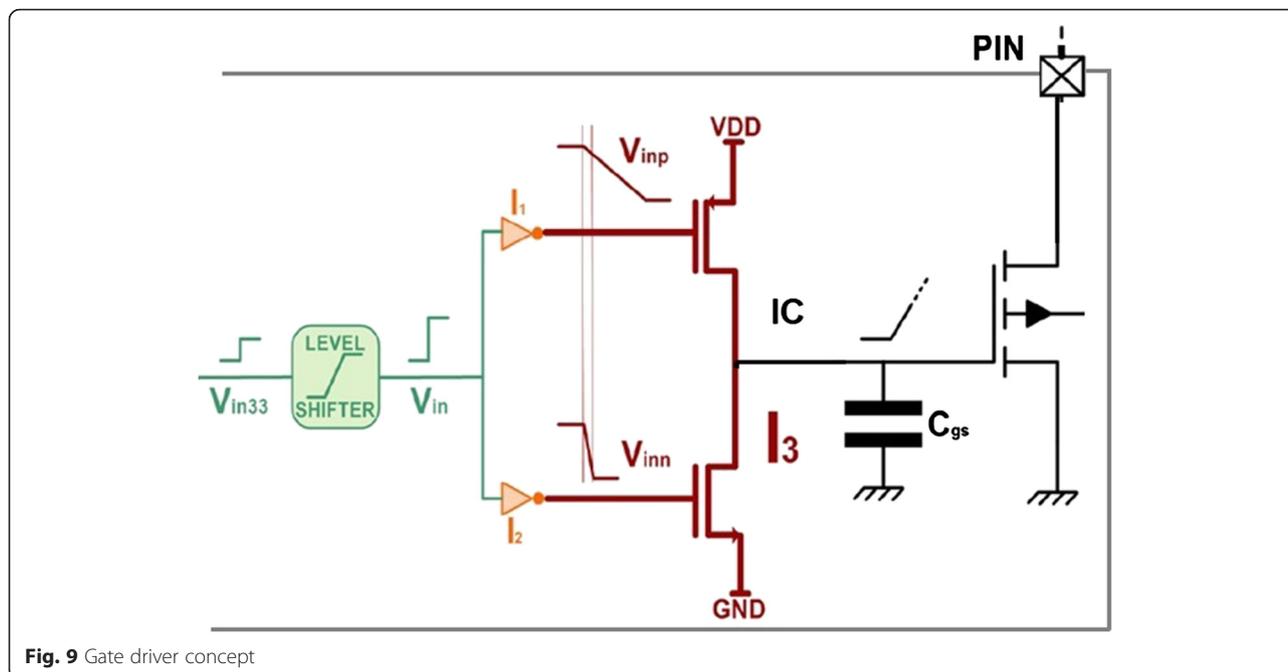


Fig. 9 Gate driver concept

the power inverter I_3 to minimize the cross conduction. The low-side and high-side stages of I_1 and I_2 have different current capability and generate an output signal with asymmetrical rising and falling edges. When a rising edge of input signal occurs, the strong pull-down stage of inverter I_2 quickly forces the gate of the NMOS of the power inverter I_3 to ground. The power NMOS is then switched off. At the same time, the inverter I_1 begins to force to zero the gate of the power PMOS of the inverter I_3 , to turn it on. As the low side of I_1 has a lower current capability than the low side of I_2 , the falling edge of the gate of the PMOS of I_3 is smoother and when it is low enough to switch the power PMOS on, the power NMOS is already off. The cross conduction of the power inverter (I_3 in Fig. 9) during the falling edge is minimized in the same way. In this structure, only the low power inverters I_1 and I_2 are affected by cross conduction, but as a low current flows through these devices, this effect has no impact on the performance of the DC/DC converter. The final stage of the gate driver, instead, is significantly improved because its cross conduction is strongly reduced and the correspondent dangerous current spikes are eliminated.

3.4 Digitally programmable output voltage

Most of state-of-the-art DC/DC converters [7–9] need an external resistive divider or a more complicated circuit to set the output voltage value. In most cases, once the output voltage is set, it cannot be changed anymore. In our design, instead, a digitally programmable resistive divider is integrated on-chip, see PRD block in Fig. 5. Using an integrated digitally programmable divider to generate the feedback

signal for the regulation loop of the converter saves costs and area on the PCB and allows changing the output voltage level in a range between 1 and 48 V at any time.

3.5 Diagnostic block

Safety has a primary role in the design of automotive ICs. These devices, in fact, must be able to prevent harms to the outer systems if a fault condition occurs [19]. In our design, a dedicated diagnostic block was implemented to detect and manage the following failures: (i) overcurrent into the primary side; (ii) overtemperature; (iii) undervoltage on the output pin; and (iv) overvoltage on the output pin.

It is very important to monitor the current flowing into the primary side of the transformer because if it exceeds the maximum allowed value (dependent on the external parts used), the external switch may be damaged and the magnetic element's core may saturate, irreversibly compromising the functionality of the whole system. When an overcurrent condition occurs, the power FET is then immediately switched off. An integrated temperature sensor generates a voltage proportional to the temperature of the die. The system manages the overtemperature by switching the converter off as soon as the output voltage of the sensor exceeds a threshold corresponding to the maximum operating temperature. Undervoltage and overvoltage conditions on the output pin are detected by comparing the reference voltage from the bandgap to two dedicated additional partitions of the output voltage. If such a condition occurs, the DC/DC is switched off.

3.6 Dithering of the switching frequency

The dithering of the switching frequency was implemented to improve the performance of the converter in terms of electromagnetic emissions. If the switching frequency is constant, the power spectrum of the system is concentrated at this frequency reaching a very high level, not compliant with automotive regulations. The technique of the dithering consists in slightly changing the switching frequency. This allows spreading the power spectrum on a wider range of frequency, thus reducing emission peak value, according to automotive regulations. Once the programmable switching frequency f_{SW} is set, the dithering function periodically changes the switching period according to a triangular law, see Fig. 10, in a range from the nominal value f_{SW} minus 12.5 % to the nominal value f_{SW} plus 12.5 %. The nominal switching frequency f_{SW} can be set at $f_{SW1} = 444$ kHz or $f_{SW2} = 888$ kHz and is obtained by dividing with a factor $n_1 = 16$ or $n_2 = 8$ a high frequency clock of about 7 MHz, used by the digital part of the integrated circuit. This keeps the mean switching frequency equal to the set nominal value, but the maximum value of the power density spectrum is reduced by 20 dB according to Eq. (1), already used in literature [20]. In Eq. (1), f_{SW} is the nominal switching frequency of the controller, δ is the percentage dither about the fundamental switching frequency (between ± 12.5 % in this design), f_{DITHER} is the dither modulation rate (set at 17.76 kHz so that the dithering period is a multiple of the switching period being $f_{SW1}/f_{DITHER} = 25$ and $f_{SW2}/f_{DITHER} = 50$), n is the system clock frequency divider used by the regulator (8 or 16 in this design). By further applying a frequency hopping between 444 and 888 kHz, we further spread the emitted power whose maximum level is reduced

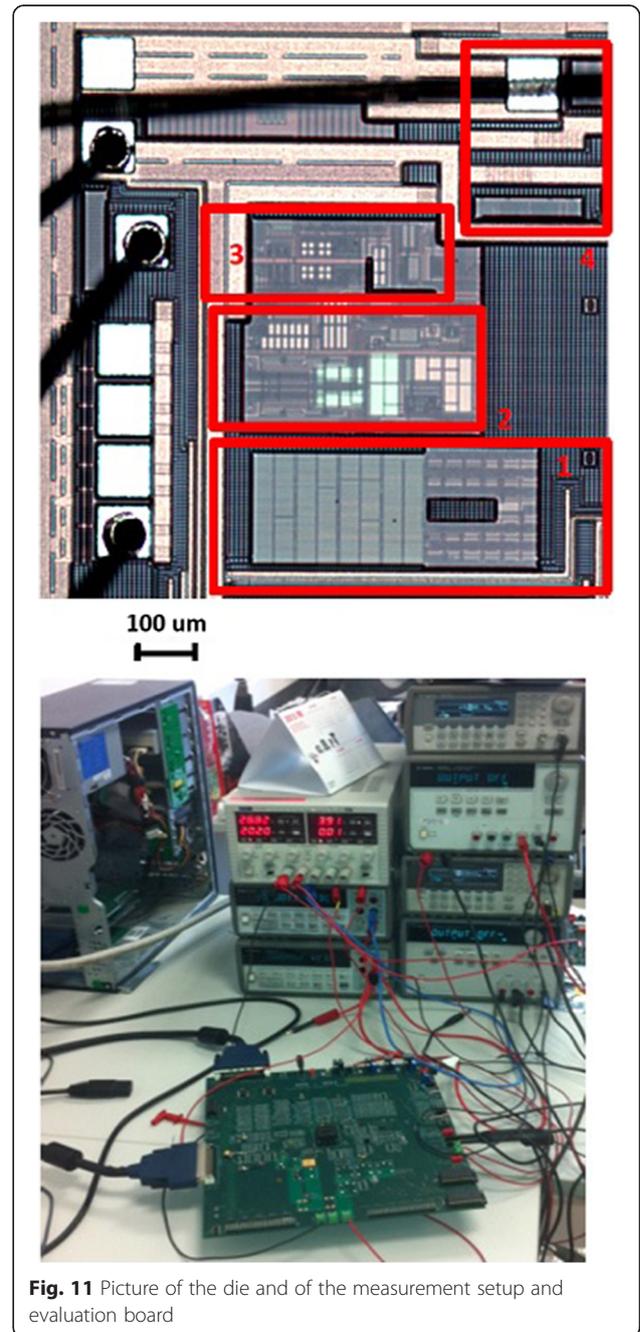
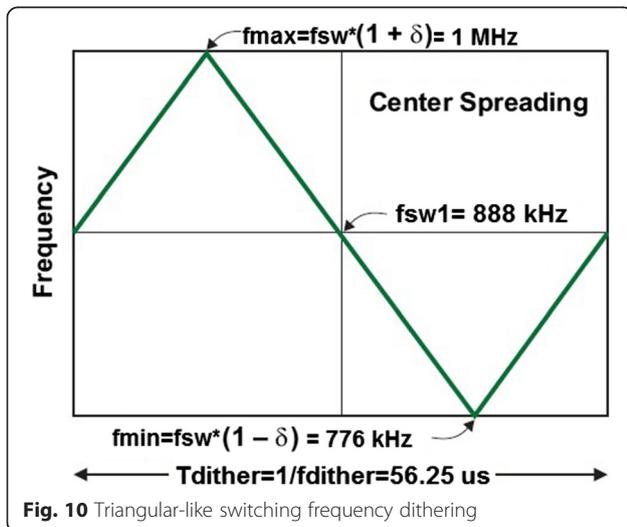
by a factor of two, i.e., a total attenuation of 23 dB of the emitted peak power level is obtained.

$$\text{Spectral attenuation (dB)} = 10 * \log[(f_{SW} * \delta) / (f_{DITHER} / n)] \tag{1}$$

4 Experimental characterization

4.1 IC characterization

The design proposed in Sections 2 and 3 was fabricated in AMS 0.35 μm CMOS technology. Figure 11 shows



the pictures of the die and the measurement setup and the testing board. The DC/DC converter integrated in Fig. 11 is part of a more complex embedded system. The blocks labelled with red boxes in Fig. 11 are the gate driver and FET, DC/DC controller, PMU, voltage divider, and diagnostic unit of Fig. 3.

During the evaluation of the IC, the performances of the DC/DC converter were fully characterized. The test setup includes a dedicated evaluation board, designed to communicate with the IC through the digital serial bus and to measure the parameters of the DC/DC converter in all operating conditions. The serial communication protocol and the automation of the measurements to be implemented were managed with a dedicated LabVIEW software and DAQ board. Most relevant measurements are presented in Tables 1 and 2. The waveforms in Figs. 6, 7, and 8 and in Figs. 12, 13, and 14 have been experimentally measured through the prototyping system in Fig. 11.

High stability margins of the system are confirmed by the smoothness of the start-up transient and of the step responses. The dynamic transient performance of the presented DC/DC converter was investigated by evaluating the line and load regulation as shown in Fig. 12. Note that if a step of 100 mA occurs (blue waveform), the output voltage (yellow waveform) does not change. The oscilloscope snapshot in Fig. 13 shows the achievement of the dynamic updating of the output voltage by setting the digitally programmable resistive divider. The greater switching activity during the transient vs. the steady state is due to the greater power transferred to the output capacitor. The behavior of the system against temperature was evaluated repeating the characterization in the wide range of ambient operating temperature, typical of the automotive applications from -40 to 150 °C using the Thermostream TP04300A system.

Figure 14 shows the current consumption in low power mode vs. temperature (when hysteric control is activated). To be noted that absolute ratings in Table 1 for temperature (-40 to 180 °C) and input voltage (-0.3 to 70 V) are larger than the operating ratings in Table 2,

since the IC has extended working ranges where the correct functionality is not guaranteed but it is protected by any damages.

After the evaluation, the qualification phase of the device took place. This activity aimed to test the robustness, the reliability, and the compliance of the designed system with requirements typical of harsh automotive environments. The system was verified to work inside the safe operating area (SOA) with lifetime acceleration factor close to 1 to maximize the mean time to failure of the device. Other typical requirements that an IC for automotive applications must meet are about ESD and latch-up. During latch-up tests, hundreds of milliamps of current are sunk by every pin of the device. This analysis guarantees that no bipolar parasitic structures will turn on during the operating life of the device. This test is very important because if such a fault occurs the device can be irreparably damaged. Electrostatic discharge tests, instead, aim to reproduce ESD events stressing the device with the application of a current pulse, obtained by discharging a pre-charged capacitor through a series resistor, on every pin of the integrated circuit. Different ESD tests can be performed. Different ESD models can also be used to guarantee the robustness of the circuit to different possible ESD events. In this case, we focused on the human body model (HBM). It aims to simulate ESD events due to the interaction of the device with the human body. A 100 pF capacitor (pre-charged at thousands of Volts) is discharged on a pin through a 1.5 k Ω series resistor. The device is tested before and after the ESD stress. By comparing the results, it was verified that no shifts of the parameters of the converter occurred during the stress. The DC/DC converter IC meets 4 kV ESD requirements. EMC is another hot topic in automotive ICs validation [21]. Special tests were performed at vehicle-level in an anechoic chamber, where a car equipped with our IC must keep working when exposed to electrical fields up to 700 V/m. The endurance to high temperature and to thermal stress was checked out by (high-temperature operating life (HTOL) qualification. The achieved performance makes the IC suitable not only for automotive, but also for applications in other transport applications such as motorcycles [22].

Table 1 IC rating for a 36 W output power

	Min	Typ	Max
Efficiency	–	85 %	–
Line regulation	–	0.01 %	–
Load regulation	–	0.13 Ω	–
Thermal drift	–	0.2 mV/°C	–
Output current	–	–	0.9 A
Absolute junction temp	-40 °C	–	180 °C
Absolute input voltage	-0.3 V	–	70 V

4.2 Comparison to the state of the art

DC/DC converters proposed in literature for automotive applications still miss of flexibility. Differently from them, the DC/DC converter proposed in this paper integrates in the same smart architecture innovative features such as step-up/step-down configuration, the slope controlled gate driver, and the frequency dithering for reduced electromagnetic interference, the digital programmability of the output voltage, a low-power hysteric control for low-power consumption mode, and a

Table 2 Comparison vs. state of the art, operating conditions

	This work	[7]	[8]	[9]	[1]
Wide temp. range °C	−40 to 150	No	No	−40 to 125	−40 to 150
Converter type	Step-up/down	Step-up/down	Step-up	Step-down	Step-up/down
f_{sw} , kHz	444, 888	100	<500	300, 500	90
Input voltage, V	2.5 to 60	3.3	8 to 20	7.5 to 40	7 to 60
Output voltage, V	1 to 48	1 to 4.5	12 to 20	0.5 to 36	1.65 to 48
Digital prog. out	Yes	No	No	No	Partially
Low power mode	Yes	No	Yes	No	No
Slope control	Yes	No	No	No	Yes
Dithering	Yes	No	No	No	No
Diagnostic	Yes	No	No	Reduced	Reduced

programmable P.I. function with nested control loops in normal mode. A comparison between this work and other recent works proposed in literature is shown in Table 2. It is important to point out that Ref. [7] even if it is included in the step-up/step-down DC/DC converters category, it cannot step up the output voltage over two times the input voltage. Ref. [8] allows to dynamically changing the output voltage value by adjusting an analog voltage on a dedicated pin of the IC. This method is very restrictive for the following reasons: (i) a dedicated additional pin and a specific off-chip circuitry on the PCB are required thus increasing cost; and (ii) setting the output voltage by adjusting an analog voltage is not aligned with the current trend of automotive ECUs to make more and more use of digital interfaces and networking. Instead, the digital programmability of the output voltage also allows sharing resources such as the digital communication bus. Ref. [9] presents a low power mode, but it is not considered because in this condition, the FET is switched off and the DC/DC converter does not work, while in our design, in low power

mode, the DC/DC converter keeps working using an asynchronous hysteretic control. Ref. [1] proposes an inductorless DC/DC converter which, compared to the proposed design, has the following drawbacks: limited output programmability since only the conversion ratio (V_{out}/V_{in}) can be configured in a limited set of integer factors; missing dithering and low power modes; reduced output current capability to few hundreds of milliamps. Moreover, the works in [7–9] miss harsh environment specifications such as an extended operating temperature range, from −40 to 150 °C with our design, and extended operating input voltage range from few volts (in case of battery cranking) to maximum 60 V for emerging 48 V DC bus electric/hybrid vehicles.

5 Conclusions

This paper has presented a novel configurable DC/DC converter architecture, integrated as hard macrocell in automotive embedded systems. Realized in 0.35 μm CMOS technology, it manages a very wide operating input voltage range from 2.5 to 60 V thus regulating all

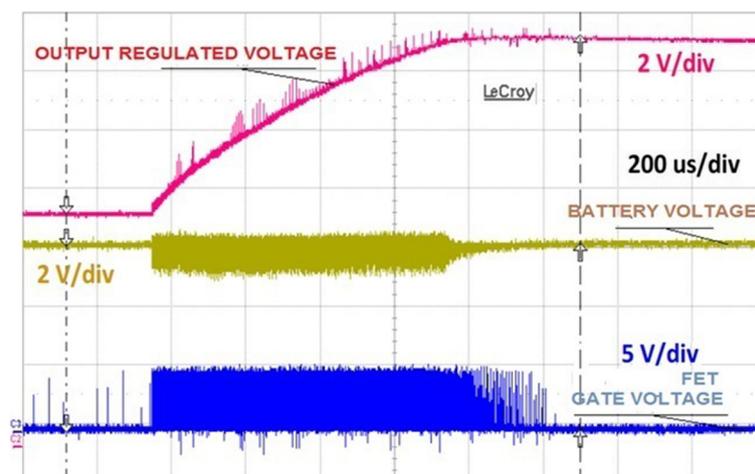


Fig. 12 Step of 100 mA on the load current, boost configuration with 8 V input and 12 V output voltages

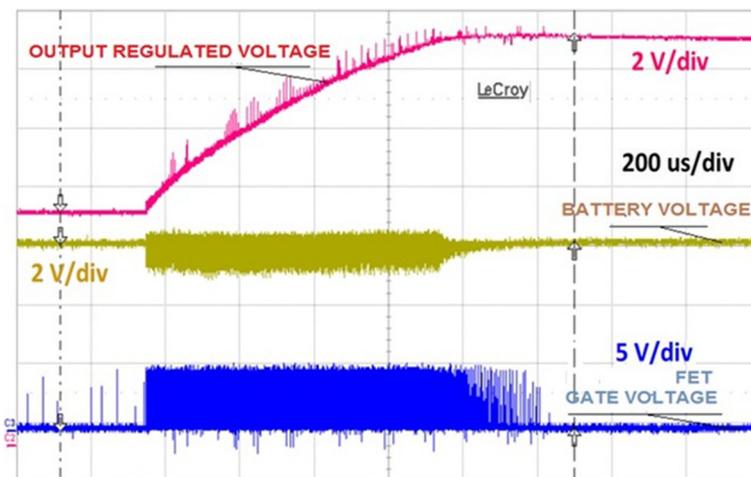


Fig. 13 Change of the output regulated voltage through LIN

voltages required in emerging hybrid/electric vehicles where, beside the conventional 12 V DC bus, also a 48 V DC bus is present. The proposed architecture realizes an intelligent converter integrating advanced features like:

- Dithering of switching frequency
- Nested control loops with both current and voltage feedbacks
- Asynchronous hysteretic control for low power mode
- Slope controlling of the power FET gate driver
- Diagnostic block against out-of-range current or voltage or temperature conditions

The converter macrocell can be connected to the in-vehicle network through LIN bus, exchanging with

the main vehicle control unit status/diagnostic flags and commands. Indeed, the proposed design supports digital configurability of the voltage, through a programmable divider, of the coefficients of the PI controller inside the voltage control loop. When compared to the state of the art, the proposed design stands for its capability of integrating in the same device all smart converter features listed above and facing harsh automotive requirements [3, 23, 24]. Experimental measurements prove that the IC can sustain automotive applications with ESD protection of 4 kV, operating temperature range from -40 to 150 °C, and up to 180 °C absolute value (the IC is not working properly but is not subject to damage), absolute voltage rating from -0.3 to 70 V. In operating mode, load current of 0.9 A can be safely managed, whereas in low power mode, the current

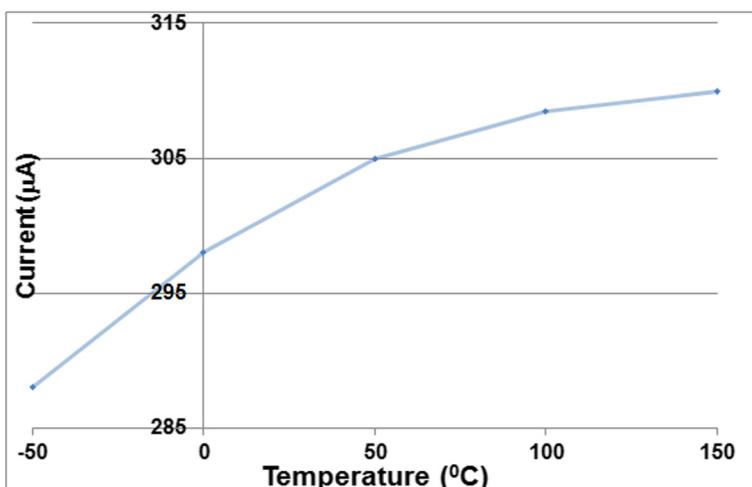


Fig. 14 Current consumption (µA) in low power mode vs. T (°C)

consumption is reduced to about 300 μA . The achieved results prove that DC/DC converters can be effectively integrated in embedded systems for mechatronic applications, facing harsh automotive conditions, and can be configured to work both in step-up or step-down modes.

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Competing interests

The authors declare that they have no competing interests.

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